CLAIMS:

What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate;

a film stack formed on the semiconductor substrate and including a film to be processed;

a dual hard mask comprising an amorphous carbon layer and an underlying hard mask layer interposed between the amorphous carbon layer and the film to be processed, said hard mask layer not including an amorphous carbon layer; and

a damascene structure for a metal interconnect formed in the film stack.

2. The device of claim 1, wherein said amorphous carbon layer comprises a part of a lithographic structure during the formation of said metal interconnect in said film stack.

3. The device of claim 1, wherein said amorphous carbon layer comprises a chemical mechanical polishing (CMP) stop layer for said damascene structure.

4. The device of claim 1, wherein said amorphous carbon layer comprises an anti-reflective coating.

5. The device of claim 1, wherein said amorphous carbon layer is configured to have optical properties that substantially match the optical properties of said film stack.

6. The device of claim 5, wherein said optical properties comprise at least one of an index of refraction, and an extinction coefficient.

7. The device of claim 6, wherein said index of refraction comprises a value ranging from 1.5 to 1.9.

8. The device of claim 6, wherein said extinction coefficient comprises a value ranging from 0.1 to 1.0.

9. The device of claim 6, wherein at least one of said index of refraction and said extinction coefficient is graded along a thickness of said amorphous carbon layer.

10. The device of claim 6, wherein said index of refraction comprises a value ranging from 1.1 to 1.9.

11. The device of claim 1, wherein said amorphous carbon layer comprises at least one of chemical vapor deposition (CVD) coating, and plasma enhanced CVD coating.

12. The device of claim 1, wherein said amorphous carbon layer is configured to provide at least one of control of a critical dimension of said single damascene structure, and control of a critical dimension variation of said damascene structure.

13. The semiconductor device of claim 1, wherein said damascene structure is a single damascene structure.

14. The semiconductor device of claim 1, wherein said damascene structure is a dual damascene structure.

15. The semiconductor device of claim 1, wherein said film to be processed comprises a low-k dielectric layer.

16. The semiconductor device of claim 1, wherein said hard mask layer comprises a nitride.

17. The semiconductor device of claim 1, wherein said hard mask layer comprises at least one of silicon nitride ($Si_3N_4$), a refractory metal and refractory metal nitride such as tantalum nitride (TaN).

18. The semiconductor device of claim 1, wherein said hard mask layer comprises a carbide.

19. The semiconductor device of claim 1, wherein said hard mask layer comprises at least one of silicon carbide (SiC) or silicon oxycarbide (SiCO).

20. A process for forming an integrated circuit structure comprising:

forming a layer of dielectric material on a substrate;

forming a hard mask layer on said layer of dielectric material;

forming a layer of amorphous carbon material on said hard mask layer; and

forming a damascene structure for a metal interconnect by using said layer of amorphous carbon material as a lithographic structure for the formation of the interconnect structure, a top layer of a dual hard mask, an anti-reflective coating, and as a sacrificial layer in a chemical mechanical polishing (CMP) process, wherein said hard mask layer is used as a CMP stop layer.

21. The process of Claim 20, further comprising:

forming a layer of light-sensitive material on said layer of amorphous carbon material, wherein the optical properties of said light-sensitive layer and said amorphous carbon layer are substantially the same;

and

exposing said layer of light-sensitive material to a pattern of radiation,

wherein said forming said layer of amorphous carbon material facilitates producing a pattern in said layer of light-sensitive material substantially the same as said pattern of radiation.

22. The process of claim 21, wherein said forming said layer of amorphous carbon material comprises depositing said layer of amorphous carbon material using at least one of chemical vapor deposition (CVD), and plasma enhanced CVD.

23. The process of Claim 20, wherein said forming a damascene structure comprises integrating an amorphous carbon layer with a single damascene structure.

24. The process of Claim 20, wherein said forming a damascene structure comprises integrating an amorphous carbon layer with a dual damascene structure.

25. The process of Claim 24, wherein said forming a damascene structure comprises integrating an amorphous carbon layer with a dual damascene structure formed using a method comprising at least one a via-first method, a full-via-first method, a full-via with no stop layer method, a trench-first method, and a buried via mask method.

26. The process of claim 20, wherein said forming said hard mask layer comprises depositing said hardmask layer using at least one of chemical vapor deposition (CVD), and plasma enhanced CVD.

27. A method of forming an interconnect structure comprising:

preparing a film stack comprising a substrate having a metal line, a metal cap layer formed on said substrate, a first dielectric layer formed on said metal cap layer, a second dielectric layer formed on said first dielectric layer, a hard mask layer formed on said second dielectric layer, a first amorphous carbon layer formed on said hard mask layer, a second amorphous carbon layer formed on said first amorphous carbon layer, and a first layer of light-sensitive material formed on said second amorphous carbon layer;

forming a first pattern in said first layer of light-sensitive material;

transferring said first pattern to said second amorphous carbon layer;

forming a second layer of light-sensitive material on said second amorphous carbon layer;

forming a second pattern in said second layer of light-sensitive material;

transferring said second pattern to said first amorphous carbon layer;

transferring said second pattern to said hard mask layer;

transferring said second pattern to said second dielectric layer;

transferring said second pattern to said first dielectric layer;

transferring said first pattern to said first amorphous carbon layer;

transferring said first pattern to said hard mask layer;

transferring said first pattern to said second dielectric layer; and

transferring said second pattern to said metal cap layer.

28. The method of claim 27, further comprising:

removing said first layer of light-sensitive material following said transferring said first pattern to said second amorphous carbon layer.

29. The method of claims 27 or 28, further comprising:

removing said second layer of light-sensitive material following said transferring said second pattern to said second dielectric layer.

30. The method of claims 27 or 28, further comprising:

preparing said film stack with an etch stop layer formed on said first dielectric layer prior to said second dielectric layer formed on said etch stop layer; and

transferring said second pattern to said etch stop layer.

31. The method of Claim 27, further comprising:

filling said first and second pattern with metal; and

chemical mechanical polishing the metal using at least one of said amorphous carbon layers as a sacrificial layer and using said hard mask layer as a stop layer.

32. A method of forming an interconnect structure comprising:

preparing a film stack comprising a substrate having a metal line, a metal cap layer formed on said substrate, a first dielectric layer formed on said metal cap layer, an amorphous carbon layer formed on said first dielectric layer, and a first layer of light-sensitive material formed on said amorphous carbon layer;

forming a first pattern in said first layer of light-sensitive material;

transferring said first pattern to said amorphous carbon layer;

forming a second dielectric layer on said amorphous carbon layer and said first pattern;

forming a hard mask on said second dielectric layer;

forming a second amorphous carbon layer on said hard mask;

forming a second layer of light-sensitive material on said second amorphous carbon layer;

forming a second pattern in said second layer of light-sensitive material;

transferring said second pattern to said second amorphous carbon layer;

transferring said second pattern to said hard mask;

transferring said second pattern to said second dielectric layer;

transferring said first pattern to said first dielectric layer; and

transferring said first pattern to said metal cap layer.

33. The method of Claim 32, further comprising:

filling said first and second pattern with metal; and

chemical mechanical polishing the metal using said amorphous carbon layer as a sacrificial layer and using said hard mask as a stop layer.

34. A method of forming an interconnect structure comprising:

preparing a film stack comprising a substrate having a metal line, a metal cap layer formed on said substrate, a first dielectric layer formed on said metal cap layer, a hard mask formed on said first dielectric layer, an amorphous carbon layer formed on said hard mask layer, and a first layer of light-sensitive material formed on said amorphous carbon layer;

forming a first pattern in said first layer of light-sensitive material;

transferring said first pattern to said amorphous carbon layer;

transferring said first pattern to said hard mask layer;

transferring said first pattern to said first dielectric layer;

transferring said first pattern to said metal cap layer;

removing said amorphous carbon layer;

filling said first pattern in said first dielectric layer and said metal cap layer with metal;

forming a second metal cap layer on said film stack;

forming a second dielectric layer on said second metal cap layer;

forming a second hard mask layer on said second dielectric layer;

forming a second amorphous carbon layer on said second hard mask layer;

forming a second layer of light-sensitive material on said second amorphous carbon layer;

forming a second pattern in said second layer of light-sensitive material;

transferring said second pattern to said second amorphous carbon layer;

transferring said second pattern to said second hard mask layer;

transferring said second pattern to said second dielectric layer; and

transferring said second pattern to said second metal cap layer.

35. The method of Claim 34, further comprising:

filling said second pattern with metal; and

chemical mechanical polishing the metal using said second amorphous layer as a sacrificial layer and said second hard mask as a CMP stop layer.

36. The method of claim 29, further comprising:

preparing said film stack with an etch stop layer formed on said first dielectric layer prior to said second dielectric layer formed on said etch stop layer; and

transferring said second pattern to said etch stop layer.